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High Speed Low Power Buffer Amplifier for TFT-LCD Application

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ABSTRACT: The proposed buffer achieves high-speed driving performance, draws a small quiescent current during static operation and offers a rail-to-rail common-mode input range. A low power rail-to-rail class-AB buffer is used to amplify the input signal difference and supply the bias voltages for the output stage. Post-layout simulations show that the proposed buffer can drive a 1-nF column line load within 0.6- s settling time under a full voltage swing, while drawing only 3.5- A static current from a 3-V power supply.

Keywords: TFT, LCD, Class AB.

I. INTRODUCTION

The charismatic development of electronics made living in nowadays almost impossible without electronic devices such as smart phone, television, and tablet. Progress in demands of human nature has forced science to grow up in this field [1, 2]. Display is a common factor among these devices, which helps so much in improving the progress of them. The main reason for users and market demand of progress in this field is that the display devices directly interface with the users. There are several improvements in this field, which can be categorized in two groups: (a) improvement in the circuit components, and (b) improvement in the hardware of displays. Buffer amplifiers are main part of the screens. They directly affect power consumption, settling time, speed, bandwidth and other parameters [3-7]. Developments in integrated circuit technology, particularly circuits related to displays & their improvements, indicate that there is a need to have a high-quality and high-speed circuit under low voltage source & low power consumption [3-7]. Recently, the technology & consumer tendency are portable devices such as cell phone and tablet. In this process, many attempts have been done to improve the circuits to achieve the objectives that generally focus on parameters such as the slew rate, voltage swing, bandwidth, maximum load current and low power consumption [3-7].

There are many attempts to increase the performance of displays such as [5-10]. In [6], the designed circuit works well in terms of charging and discharging speed of large capacitors, but it has low bandwidth. In [7] and [8], the designed circuits have a good bandwidth, but they do not have the ability to charge large capacitors well. In [9] developed circuit works well in terms of charging and discharging speed for relatively large capacitors, but it has a relatively high power consumption. The developed circuit in [10] works well in terms of charging and discharging speed of large capacitors. The power consumption is also relatively good, but it has low bandwidth. This paper presents a low power high speed buffer amplifier for TFT LCD. The proposed buffer amplifier consist.

The circuit provides enhanced slewing capabilities with limited power consumption by exploiting two current comparators embodied in the input stage, which sense the input signal transients to turn on the output stage transistors [4-5].

CMOS devices have a high input impedance, high gain, and high bandwidth. These Characteristics are similar to ideal amplifier characteristics and, hence, a CMOS buffer or Inverter can be used in an oscillator circuit in conjunction with other passive components. Now, CMOS oscillator circuits are widely used in high-speed applications because they are economical, easy to use, and take significantly less space than a conventional oscillator [3-7].

II. PROPOSED BUFFER AMPLIFIER

The LCD output buffers are mostly realized by operational trans-conductance amplifiers in unity gain configuration, and are typically used to drive the highly capacitive column lines of the display panel. Moreover, as a high open-loop gain is required to obtain a low-valued systematic offset voltage, two-stage amplifier architecture is traditionally adopted in the LCD driver. However, to provide high speed driving capabilities to the output stage, a few additional current comparators are usually included in the basic two-stage amplifier topology, hence requiring some extra quiescent current from the power supply.

This work suggests a new compact low-power rail-to-rail class-AB Buffer amplifier for large-size LCD applications. The proposed buffer provides a remarkable power efficiency improvement compared to other previously reported solutions, as both current comparators are freely incorporated into the input differential stage [1]. The transistor-level implementation of the proposed output buffer is illustrated in Fig.1. and the Fig. 2 shows Layout diagram or given circuit. As a unitary-gain amplifier, V_{out} is connected to the inverting input V_{in-}, while the input signal is applied to the non-inverting terminal V_{in+}.

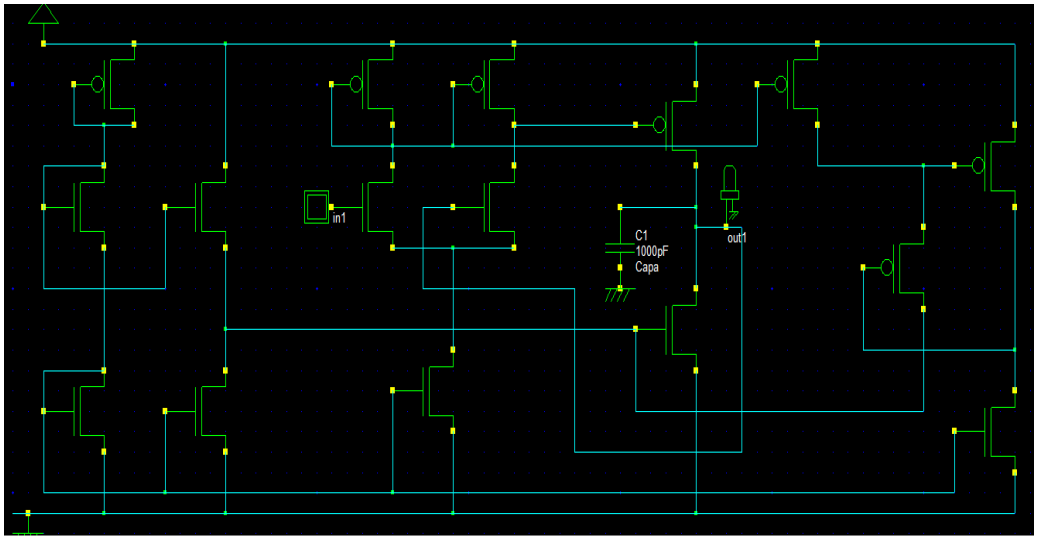

Fig. 1. Circuit diagram of the buffer.

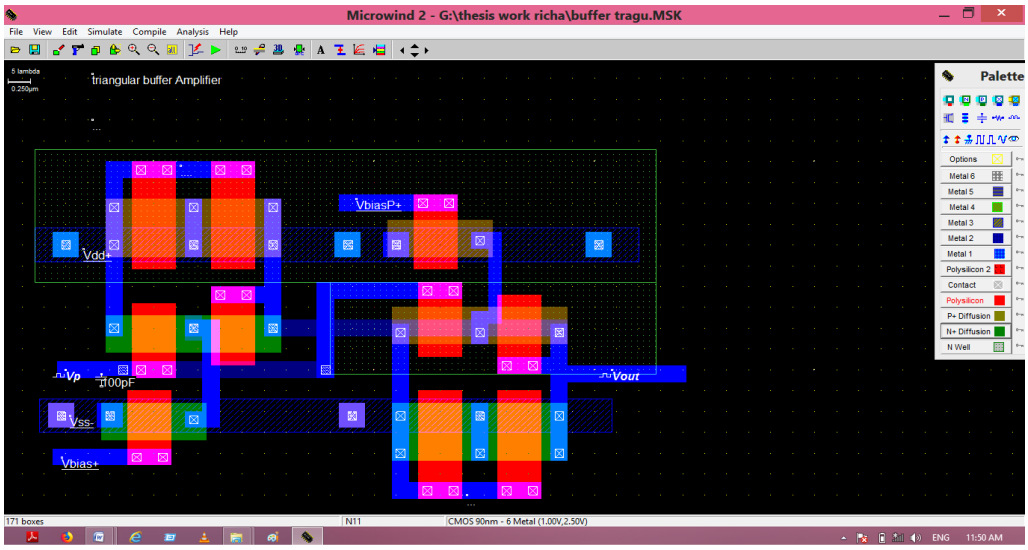

Fig. 2. Layout diagram of the main buffer implemented.

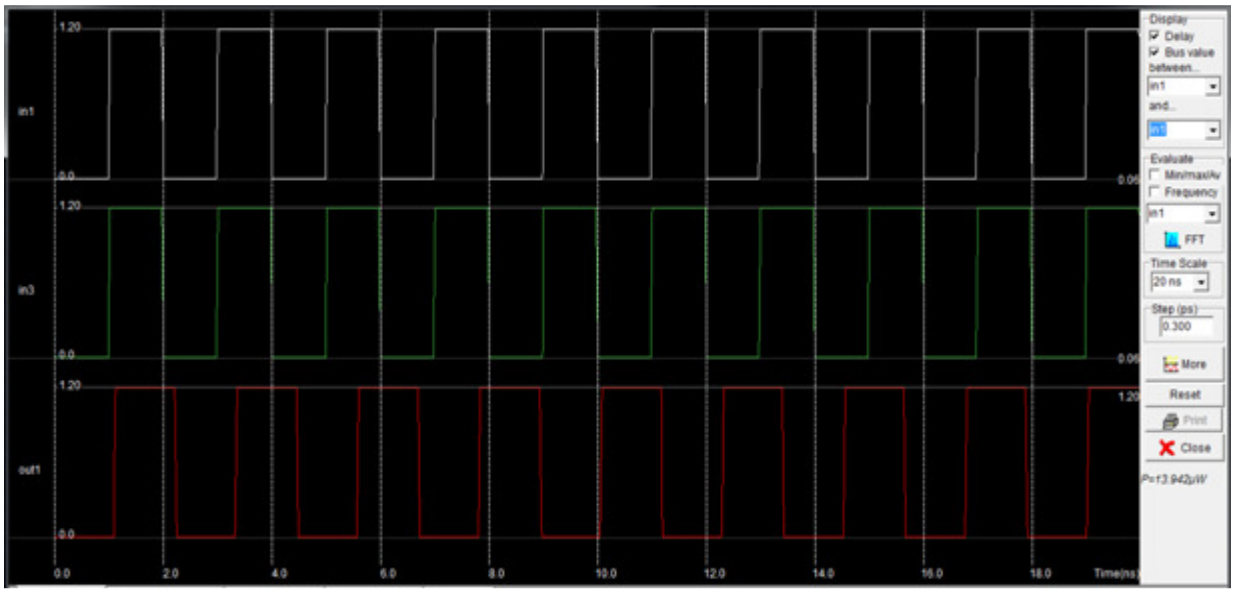

Fig. 3. Output waveforms of the voltage at buffer.

It should be noted that figure 1 depicts output power stage. To ensure the other driving devices MO1 and MO2 to stay off during static operation and to save power consumption, the DC currents of MC1 and MC4 are designed to be slightly lower than the nominal currents of MC2 and MC3, respectively. The above specification is fulfilled by the following design conditions:

$$\frac{(\frac{W}{L})_{MC1}}{(\frac{W}{L})bias_p} = \frac{(\frac{W}{L})_{MC2} - \Delta(\frac{W}{L})}{(\frac{W}{L})bias_n}$$

The fig 3, 4 & 5 shows some important result wave forms & fast fourier transform response for output of circuit with validation of proposed work by compression Table 1.

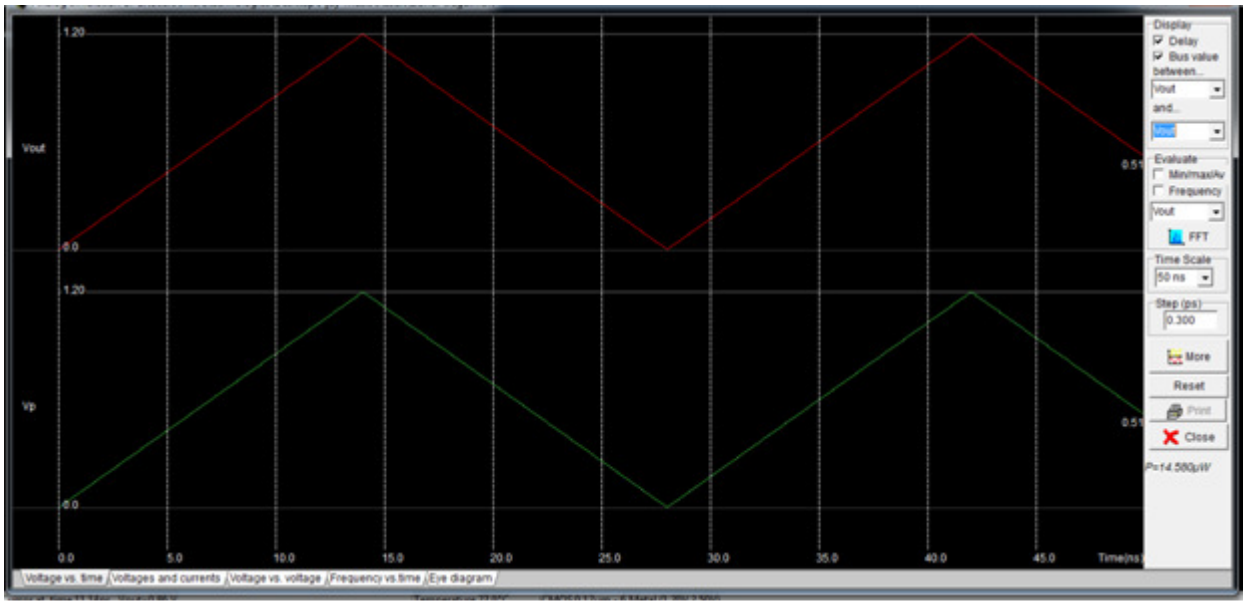

Fig. 4. Output waveforms of the voltage at varying load capacitor's value.

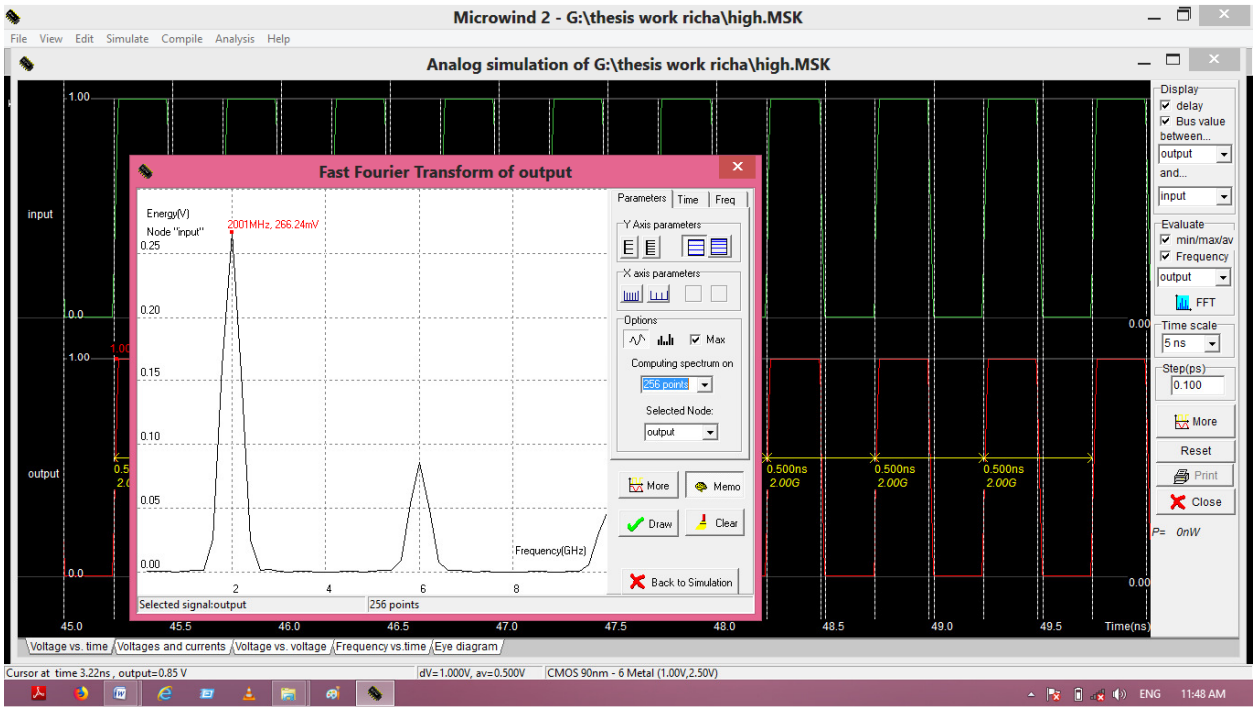

Fig. 5. Input and output waveforms of the voltage with their frequency response.

Table 1: Comparison Table.

	Ref.[10]	**Ref.[15]**	**Ref.[17]**	**Ref.[1]**	**This work**
CMOS TECHNOLOGY	0.8µm	0.35µm	0.35µm	0.6µm	0.6µm
OPERATION CLASS	B	B	AB	B	AB
SUPPLY VOLTAGE (V)	5	3.3	3.3	3	3
LOAD CAPACITOR (pF)	600	600	1000	1000	2000
QUIESCENT CURRENT (µA)	24	7	7.7	3.5	4
SETTLING TIME (µs)	5.5	2.8	1.28	1.7	0.6
IN/OUT RANGE (V)	80%	100%	100%	100%	82%
ACTIVEAREA (µm^2)	230*140	46*58	25*25	30*30	21*27
POWER DISSIPATION (mW)	NA	NA	NA	NA	1.493 µW
SLEW RATE (V/µs)	NA	NA	NA	NA	12V/µs

III. CONCLUSION

It is limpidly visually perceived in the results that the output waveform follows the input waveform. Withal the comparison table depicts a remarkable amelioration of the proposed amplifier over other antecedently reported buffers. Hence the high speed self inequitable low power rail-to-rail class-AB buffer amplifier is implemented prosperously.

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